AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0006], page 2 lines 16-26, with the following:

In conventional semiconductor devices consisting of multiple blocks, some or all of the blocks have independent clock circuits, each of which drives a clock signal used within each block in accordance with a clock signal provided from a common clock generator circuit provided for the multiple blocks. However, when a clock signal is driven within each block, clock skew can occur within each block due to timing disagreement in driving the clock signals in the blocks. Such clock skew between blocks ~~occurs~~ can cause a problem of disagreement in signaling timing between blocks. Therefore, semiconductor devices consisting of multiple blocks use a delay circuit to adjust the timing of a common clock signal inputted into the blocks to control clock skew between the blocks.

Please replace paragraph [0008], page 3 lines 9-13, with the following:

Clock generating circuit 10 generates a clock signal and supplies it to blocks 31 and 32. The clock signal supplied from clock generator circuit 10 to block 32 is delayed by delay circuit 120 inserted between them, and a clock delayed by a certain amount of time from the clock signal generated by clock generator circuit 10 is provided to block 32 as its clock signal.